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Project Information			
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Start Date	April 2009	**End Date**	April 2010
Lead Institution	University of York		
Project Director	Dr Chris Crispin-Bailey		
Project Manager & contact details	As above, chrisb@cs.york.ac.uk		
Partner Institutions	n/a		
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Document History		
Version	**Date**	**Comments**

1. Title Page

Java Bread Board Tools

Department of Computer Science, University of York

FINAL REPORT

Dr Chris Crispin-Bailey
Dr Michael Freeman

2. Table of Contents

3. Acknowledgements

This project was funded by the Academy and JISC under the OER programme (individual Strand). Work undertaken on the project was carried out by Dr Michael Freeman and Dr Chris Crispin-Bailey. Work was built upon previous work by University of York Project Students, including Nicholas Glass, Shaun Gilbert, Stephen Halstead, and Rob Page.

4. Executive Summary

The aim of 'Java Bread-Board' as an OER project, was to take an existing set of software tools (developed at York University) and undertake the necessary work to make them available as an open-source and open-learning toolset. The idea is that educators can develop new learning materials and modules , based upon the JBB tool-set as a learning environment, and in another instance and educator or student could develop extensions to the software itself, increasing its applicability to curriculum areas and adding new features to support learning outcomes.

By Open-Source we mean the software itself may be altered and extended to new purposes by third parties , under a non-profit licence arrangement. By Open-Learning , we mean that the Tools will be available without costs for non-commercial learning activities and private study.

In order to provide a complete outcome under the open-learning resources goal, the software is to be released along with some initial learning materials, with the intent to expand these through our own efforts and contributions from the community of users and educators.

In technical terms, work has been conducted on the source code (written in JAVA) for the Bread-Board simulator. The reasons for undertaking this work were (a) to improve upon certain usability issues that existed in the previous software tool-set, (b) improve the interface for third-party developers of new modules for the Tool set, and (c) to ensure future development and maintenance can be effectively carried out.

The outcomes of the project are as follows:-

1. The source code has been prepared for open source release
2. The source code has been rationalised to support third-party development
3. The tools have been modified to overcome minor usability issues.
4. Two sets of learning materials have been developed.
5. Depositing of the Software tools on Jorum[1]
6. Depositing of the learning materials on Jorum[2,3]
7. Depositing of source code on a platform, e.g. Source-Force, for community access.
8. Establishment of a permanent web presence and community[4]

[1] http://deposit.jorum.ac.uk/mod/resource/type/mrcuteget/preview.php?directory=/JorumOpen/Java_BreadBoard_Tool-Set_v1.10_334_30-04-2010

[2] http://deposit.jorum.ac.uk/mod/resource/type/mrcuteget/preview.php?blockmode=1&directory=/JorumOpen/Java_BreadBoard_Introductory_Digital_Exercises_334_04-05-2010&choose=id_reference

[3] http://deposit.jorum.ac.uk/mod/resource/type/mrcuteget/preview.php?blockmode=1&directory=/JorumOpen/Java_BreadBoard_CPU_Exercises_334_04-05-2010&choose=id_reference

[4] www.cs.york.ac.uk/jbb

5. Background

Summarise the background to the project and the need it for it (and why it's important) in the context you are working in. This should include brief clear summaries of:

a) Where your project fits within the OER programme (strand, topic focus, key issues addressed)

The Project was an individual strand project , with a focus upon making open learning resources available, namely the digital electronics tool-set. The project delivers a stable open-learning resource to enable digital electronics teaching to move from pure theory to experimental-learning scenarios, without assuming that learners will have access to suitable resources (as the Toolset provides these for free to anyone who wants them).

The project also seeks to develop a user-developer community model, whereby learners and educators are free to develop extensions to the tool-set for their specific purposes, provided these are also open-source and open-learning releases on a non-profit basis. It is hoped that this will encourage new features and resources to be developed, extending the toolset in ways which the current team cannot practically undertake with limited resources.

b) What the state of OER release and resource sharing more generally was, in your project's domain, prior to the start of your project

The JBB toolset prior to the OER project was only partially available in the public domain. Several components of the system were not up to the required standard for release. However there was evidence of JBB being used widely in this limited form.

The Source code was not officially available, and was not considered to be in a state that would allow effective open-source community involvement. A number of unofficial mirrors site had been set up without our agreement, and the user community was fragmented.

c) How your project built on previous work and/or exploited specific opportunities in your domain

The previous work exploited in this project is primarily that of which we have conducted internally in the past 6 years. A number of student projects were used as a vehicle for developing the JBB tool-set to an extent that it could be used internally. However, the work required to make the tools suitable for OER release and open source exploitation was not suitable for project work, and couldn't be justified without the OER support to fund the effort of the actors within the project (particularly Dr Freeman).

d) *How your project proposed to advance OER release and why this was important to your stakeholders*

The objective of the JBB project was to make available the JBB tool-set in such a way as to allow both it's wide use as a learning enabler for digital electronics, and also its use as a platform for development of further learning tools in an integrated environment without commercial constraints.

We are not aware of a tool that provides the same functionality as JBB, and as a free resource, its use is not constrained by the budget constraints of individuals, educators, or institutions. A second point of interest is that the tools follow the 'Bread-Board' model of circuit prototyping very closely. This is a model which relates to physical circuit building in teaching labs particularly, so the tool provides a supplement or substitute to this lab-based activity, though the philosophy is that the tools are ideally in addition to rather than instead of a physical lab experience.

This provides the broadest opportunity for its uptake, from individuals to schools, colleges, and universities, and also means that its use is possible, in less-developed countries where educational resources are limited. Importantly, the software itself is based upon JAVA, a language that provides platform independence – in other words, the computer upon which the software runs may be a basic PC, apple mac, laptop, with Windows, Linux , and other operating systems. The OLPC ($100 laptop) community is providing increasing support for JAVA, making it possible to envisage use of JBB in this context – this may be an area to follow up after the OER project is completed as it would be relatively inexpensive to conduct some testing and ensure compatibility issues are identified and addressed at some point.

6. Aims and Objectives

There were no changes to the project plan. The key objectives were as follows:

6.1 Open Educational Resources to be released

The following resources were to be released:-

1. Java Bread-Board Main Tool and associated plug-in tools
2. Learning examples based upon introductory digital electronics themes
3. Advanced Circuit examples based upon a computer architecture topic
4. Applicable user manuals and guides for the software

5. Java Bread-Board Source Code (open source release)
6. Appropriate developers manuals/technical info to allow further development

7. Web-site presence for the open-source software and community

8. Jorum & other repository availability of Java BreadBoard tools & learning materials

Technical developments were to be undertaken:-

Limited technical work was anticipated in order to ensure that the software was satisfactory for users, and also suitably re-organised to allow easy open-source developments by third parties:-

1. Adding access to third-party plug-ins via the main menu tabs
2. Improved circuit load-save capability to allow complete circuit information to be saved (this is important when sharing examples as in a learning context for instance)

3. Improved interface points for third-party developers to define new plug-in tools and chips
4. Recompilation of the software with an up-to-date development environment, to allow easy adoption of the source code for further development.

6.2 Practices/ processes around OER to be reviewed and/or reformed

No comments.

6.3 Lessons to be learned about OER release.

The OER Release process appears straightforward in this instance. At this end-point to the project we are still in the process of continuing evaluation through the JBB community portal feedback and discussion groups. We do make some observations about the community engagement in later sections which may be relevant.

6.4 Evaluation strategy

Evaluation comes in two aspects, firstly the tools an learning materials as useable resources, but secondly the tools as an extensible platform for future development by the community itself.

The project evaluation plan was to be based upon making available the learning exercises to students during the spring and summer term. This is still our intention, but results will not be available until after the project report is submitted due to the practicalities of involving students in this process.

A longer term evaluation approach includes several members of staff in the Department, who we have encouraged to look at the tools as a possible learning platform. We will be discussing their use in the curriculum over the next few months into summer, with a view to trailing them in course materials starting in October 2010.

Additionally, the new JBB web-site at www.cs.york.ac.uk/jbb provides a full user community capability, with the opportunity for individuals to browse the site and discussion forum, or register and contribute. We expect that this can provide feedback that will be very useful for ongoing development and use in an educational context. Individuals could include tutors and students.

7. General approach

The initial expectation for deposits were primarily our own work (this is an individual strand project so limited in scope initially). However there is the possibility to engage additional staff members and encourage their work to be deposited on the Jorum site as part of our longer term aim to gain new additions to the learning material.

Our experience shows that this particular resource will be used by (a) educators – to facilitate clearly defined learning activities that are available in or out of classrooms, (b) students for self study, and (c) independent learners who are interested in curiosity driven experimentation in digital electronics.

Community engagement as an aim has not been completed yet in a substantial way – this is an ongoing activity. However, the new site is live now and will gradually acquire an enlarging user base – this has already started to happen. Additionally, dissemination opportunities have been taken up, which we believe is an important first step to broadening awareness of our tools amongst academic and educational communities (see section 8 for more info). The Jorum deposits will be referenced in our forthcoming Journal paper (accepted for publication in spring 2010 Volume)[5].

To allow uptake of the tools by the community manuals and information is provided for both users, and developers, therefore suitable information will be accessible by those who need it, in the appropriate context. Users can be taken to include students and/or educators.

Evaluation is to be continued in several ways. (a) review of materials by a qualified educator, (b) informal evaluation by students by making the developed resources available, (c) by monitoring the uptake of the open source software for development. Case (c) is a long term objective and will not be completed within the timescale of the project.

Legal issues were focussed upon the understanding of licences, and ensuring that past contributors to the project were aware of our open-source plans, and there was no doubt as to their permission for this to be undertaken.

The software has been developed over a number of years, with major contributions from final year project students. The contributors have been contacted and asked to reconfirm permission to make the software open-source. This was a precaution, as the original development of the software was undertaken on the understanding that it could be made available as open-source and open-learning resources.

[5] **Java Bread-Board :- Digital circuit simulation with an Open-source toolset, IJCSIS (International Journal on Computer Science and Information Systems** IADIS ISSN: 1646-3692. Bailey, Freeman. (Spring 2010 : accepted :- dates and final copy to be confirmed).

8. Implementation

The project followed the course anticipated in the project plan. After attending a training course on JAVA, an essential prerequisite to undertaking work on a complex java project, the initial work focussed upon technical issues, ensuring that the software would be fit for purpose (both as a learning tool and for further development). This work was successful. The second phase of the project was concerned with developing learning examples. Dr Freeman created a new set of learning exercises for the Java BreadBoard based upon his CSA course (Computer Systems Architecture). Later work concentrated upon a more advanced learning exercise based upon a simple processor built from breadboard components, illustrating a number of computer design issues.

Final work on the collation of the deposits has been completed, with work uploaded to Jorum, and addition as likely to be made in the near future.The source code will be available from Jorum if a suitable licence arrangement can be identified, but it has also been placed on SourceForge, a site dedicated to open-source code management.

Dissemination via publications have been achieved with one international conference paper and presentation (2009), and one forthcoming International Journal paper to be published in 2010 (see section 9).

Final work-packages mentioned in the draft final report have been completed, including W3b (web site content and finishing), which relates to the finalisation of our own web-space for the project, and the uploading of materials to Jorum and Source-Forge. Review of the learning materials produced was undertaken by Dr Nick Pears.

The new JBB home portal www.cs.york.ac.uk/jbb has been successfully established, and already has unsolicited sign up from new members in the community who have an interest in JBB.

9. Outputs and Results

9.1 Technical developments

The JAVA bread-Board tools provide a user interface to a circuit simulator, which will be familiar to all electronics students. A typical example of the software[6] is shown in figure 1.

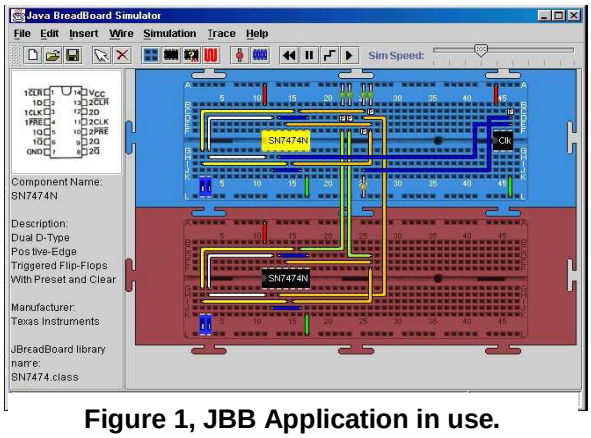


Figure 1, JBB Application in use.

The software typically entails the use of chips and wires to create circuits. A significant part the work carried out was to reorganise and update the program code associated with the ,management of chips, to allow a clear and straightforward way of managing third-party chips developed by future users.

A new hierarchical chip management scheme was developed (fig 2), to facilitate the extension of both existing chips, and addition of new ones within the same class or in a new group. Digital chips can be grouped into such categories as TTL, CMOS, FPGA, ASIC, CPU, Memory, and so-on. The hierarchy support s this. Additional groups can be added by new developers easily. Within these groups there can be almost unlimited sub-types. The new software provides a clean route to support this. This was considered essential to make third-party developments manageable.

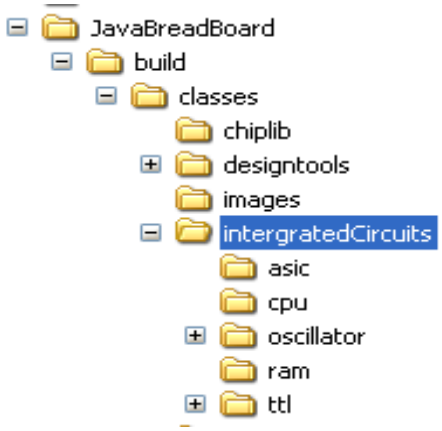


Figure 2, chip hierarchy

The final figure (fig 3) shows the approach taken to the extensible digital design input methodology supported by the adapted software. The system supports standard chips as designed by the JBB team, and any third party developers. It also supports user-defined chips, including those designed using well-known methodologies of truth-table, state-table, schematic, and HDL style.

A mechanism for new design entry tools to be built into the Java bread-Board tools menu has been implemented, to allow such extensions to be designed by third parties and integrated with the JBB tools as if they are part of the original tool-set.

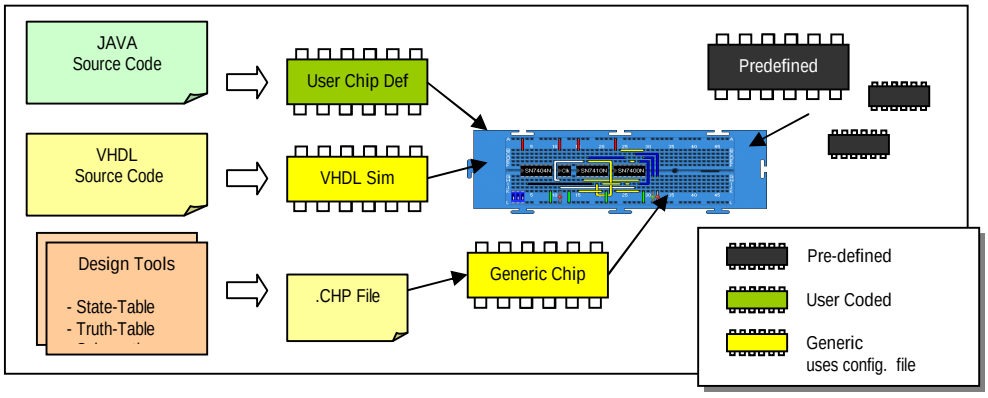


Figure 3, chip Design Methods

Open

[6] Nicholas Glass

9.2 Educational Resources released

The educational outcomes include the following:-

A. For Users Generally:

1. **The Java Bread-Board Toolset** *(executables)*, Including:-
   - Main Simulator Environment
   - Design Input tools (Truth Table, State Table, Schematic)
   - Standard Chip Libraries
2. **User Guide for the above**:-
   - 'Getting Started with Java Bread-Board' (for learners at any level)

B. For Learners:

3. **Digital Design Introductory Exercises** (year 1 degree standard)
   - Digital Circuits, Labs 1,2, and 3
4. **Advanced - CPU design Tutorial** (year 1 or year 2 Degree standard)
   - 'J Machines', Labs 1,2,3, and 4

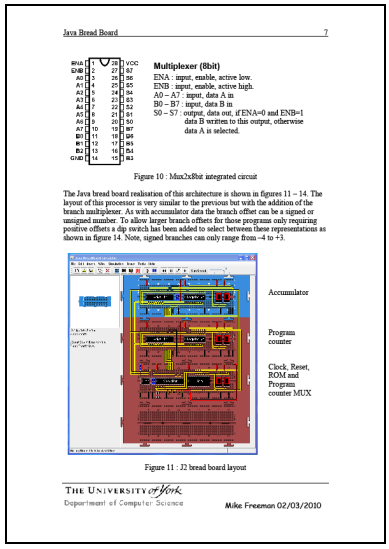
C. For Educators:

5. **Worked Examples and Tutor support materials :-**
   - resources for [3] Digital Design Introductory Exercises
   - resources for [4] Advanced Exercises

D. For Developers:

6. **Source Code release under Open-source Licence :**
   - Full JBB Toolset Source Code
   - Program Code Documentation

Example extracts from Learning Materials:


Java Bread Board 7

Multiplexer (8bit)
ENA : input, enable, active low.
ENB : input, enable, active high.
A0 – A7 : input, data A in
B0 – B7 : input, data B in
S0 – S7 : output, data out, if ENA=0 and ENB=1 data B written to this output, otherwise data A is selected.

Figure 10 : Mux2x8bit integrated circuit

The Java bread board realisation of this architecture is shown in figures 11 – 14. The layout of this processor is very similar to the previous but with the addition of the branch multiplexer. As with accumulator data the branch offset can be a signed or unsigned number. To allow larger branch offsets for these programs only requiring positive offsets a dip switch has been added to select between these representations as shown in figure 14. Note, signed branches can only range from –4 to +3.

Accumulator
Program counter
Clock, Reset, ROM and Program counter MUX

Figure 11 : J2 bread board layout

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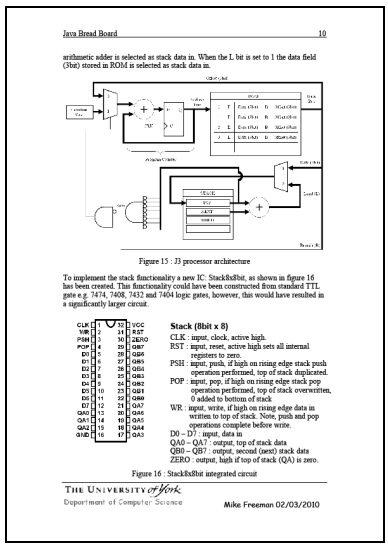
Java Bread Board 10

arithmetic adder is selected as stack data in. When the L bit is set to 1 the data field (3bit) stored in ROM is selected as stack data in.

Figure 15 : J3 processor architecture

To implement the stack functionality a new IC: Stack8x8bit, as shown in figure 16 has been created. This functionality could have been constructed from standard TTL gate e.g. 7474, 7408, 7432 and 7404 logic gates, however, this would have resulted in a significantly larger circuit.

Stack (8bit x 8)
CLK : input, clock, active high.
RST : input, reset, active high sets all internal registers to zero.
PSH : input, push, if high on rising edge stack push operation performed, top of stack duplicated.
POP : input, pop, if high on rising edge stack pop operation performed, top of stack overwritten, 0 added to bottom of stack.
WR : input, write, if high on rising edge data in written to top of stack. Note, push and pop operations complete before write.
D0 – D7 : input, data in
QA0 – QA7 : output, top of stack data
QB0 – QB7 : output, second (next) stack data
ZERO : output, high if top of stack (QA) is zero.

Figure 16 : Stack8x8bit integrated circuit

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Department of Computer Science
Mike Freeman 02/03/2010

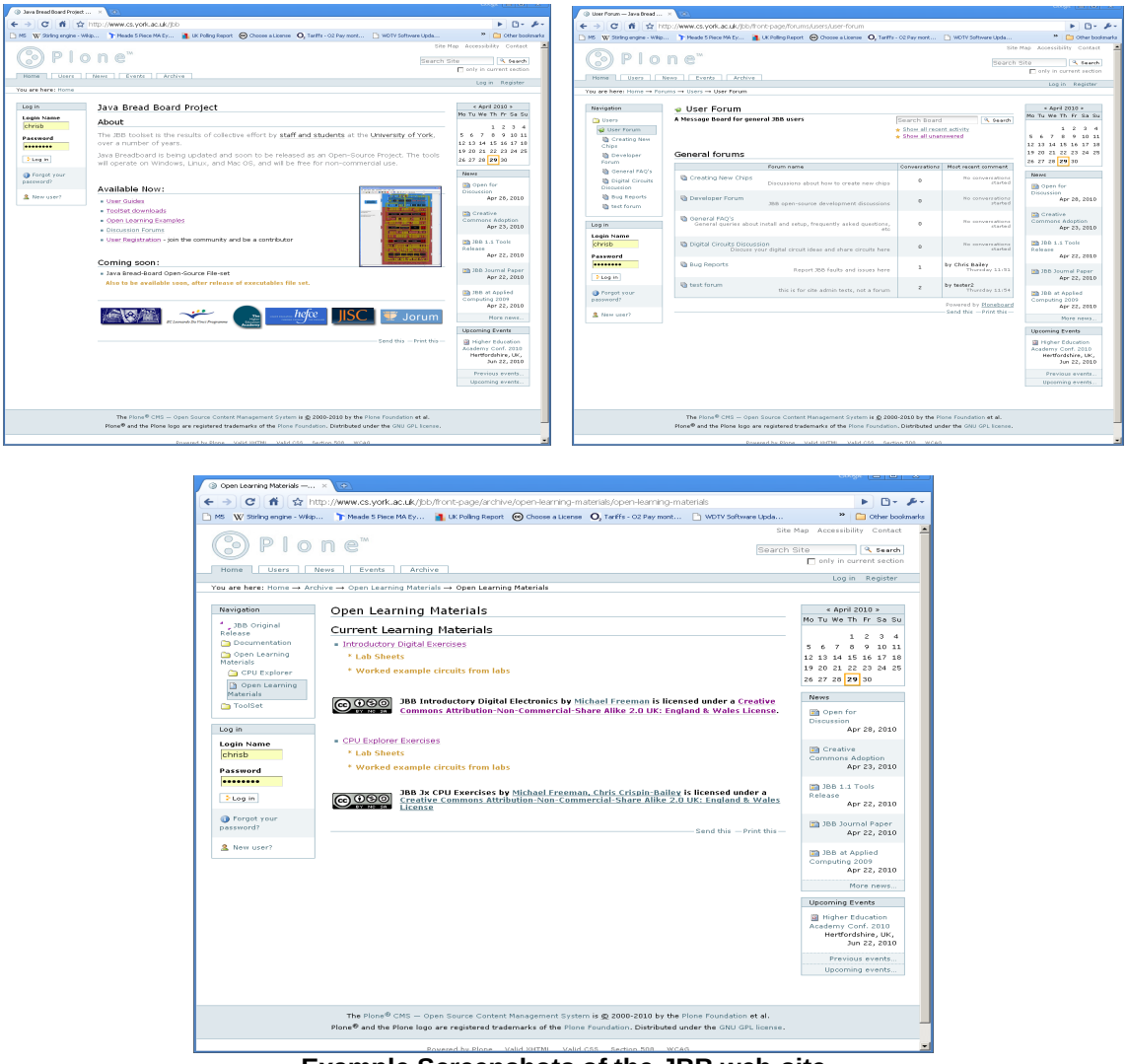
Availability of Items A,B, and C, is expected to be ensured via Jorum in the first week of March 2010, whilst the developer resources (D) will be placed on Source-Forge and possibly Jorum (if deemed appropriate), in a similar timescale. In addition, a web-site[7] dedicated to the JBB tool-set is being

[7] www.cs.york.ac.uk/~chrisb/projects/jbb

completed, which will include links to all of these resources, and may eventually provide a community support function via news-groups etc.

Online Deposits/Presence.

The Java Bread-Board project now has a dedicated web-site for the user community. This can be located at www.cs.york.ac.uk/jbb



Example Screenshots of the JBB web-site

This site provides some key resources, in particular:-

- A download archive for JBB tool-set releases
- Access to open-learning materials based on the JBB OER project (Creative Commons Licensed and branded)
- A discussion forum for users including ability to post circuit designs as contributions or discussion points.
- A discussion forum for developers wanting to extend JBB

These can be seen more clearly by visiting the site at the url provided. Visitors can register and access the full site facilities, or browse as a casual user. A number of people have already registered.

9.3 Innovations in practices/ processes around OER

Again describe these with reference to any institutional documentation

No comments.

9.4 Guidance on OER release and associated issues and processes.

Please list events, workshops, consultations etc held, and any guidance materials produced, as well as any evidence of uptake

No Comments

9.5 Dissemination outputs

At this stage our dissemination has resulted in a conference publication ("**A JAVA Bread-Board Simulator : Digital Circuit Simulation with an Extensible Learning Tool"**, Proc. of **IADIS 2009** Applied Computing Conference, pp___, Rome, 2009, Chris Bailey, Michael Freeman., see also appendix 1) and a forthcoming Journal Paper publication ("**Java Bread-Board :- Towards an Open Source Future", IJCSIS** (International Journal on Computer Science and Information systems IADIS ISSN: 1646-3692. Bailey, Freeman. (accepted :- dates and final copy to be confirmed).) .

9.6 Outputs from the evaluation process

Evaluation studies will be posted on the JBB site in future, at www.cs.york.ac.uk/jbb

Evaluation Outcomes

One particular example that is worth noting is the recent activity within our department in reformulating curricula in advance of introduction of new modular degree programmes (Oct 2010). A number of staff in the digital electronics domain have been working together on revising and restructuring the digital electronics curriculum content. It was noted that having an equivalent capability in JBB tools to those in our own labs would be very useful for teaching purposes. As a result we started a new final year student project, during the OER project, which will provide the ability to include specific FPGA/CPLD chips that are to be used in the real lab-work. We are now hoping to use JBB in several parts of the 1st year curriculum as a common study tool.

10. Outcomes and Impact

The improving capabilities of the tools have already created some interest within the university. Fellow educators have expressed an interest in using the software for their own learning objectives. This has allowed further student-projects to be initiated that will create new resources for use with the tools that align with these other modules.

The wider release of the software is ongoing at this stage, the JBB portal has already allowed dissemination and feedback to be undertaken, and a new revision of the software has been released recently.

What do you think the critical success factors were for achieving the impact you have achieved?

It was relatively easy to ensure stakeholder consent was confirmed by the individual students that contributed previously, as they had been informed during their respective projects that the

work could eventually be released as an open resource. Not all universities have a clear IP ownership policy for student work, and even if it is believed that there is one in place, a sensible advisement would be for those developing education software in the same way to define from the start the intention for open resourcing, to keep the option clear for future exploitation.

What do you think the critical barriers to achieving impact?

This comment possibly relates more to future impact: One of the issues we have encountered is the issue of developing a user community using appropriate technical tool such as discussion groups. Although these facilities are of course widely available and technically do not present problems, the issue is of ownership – if a university employee sets up a discussion group then the university is ultimately responsible for its content, and this would imply a level of monitoring and support that could not be justified or supported. It would make the university legally responsible to ensure that the user forum does not contain anything illegal or defamatory in nature.

It should however be less problematic to establish a closed forum, which UK academics can join. This is also an area we may investigate in the future.

If Jorum were able to provide a facility to set up discussion threads aligned with each Jorum Deposit, this would remove a significant obstacle for wider engagement with the potential user community. The idea being that the community would ideally 'help itself' by virtue of the discussion process, and occasional input from experts.

11. Conclusions & Recommendations

The most interesting aspect of this project, which may be a little different to others in the OER programme at present, is that it seeks to develop and deposit something dynamic. In other words, the end result is not a final piece of work for future reference, but actually a set of tools, and learning examples which can be continually developed . The learning materials can be added to by third parties simply by basing them around the Java Bread-Board tools, ideally following a similar style to those already deposited. The tools themselves can be extended and added to create new opportunities and customisations to allow uses beyond their original intent, or to ensure they remain up-to-date in terms of current methodologies in the digital design field.

It would be interesting if Jorum could support this style of deposit in a more structured way, by for instance creating a discussion forum and collective contribution capability linked to a group of deposits which can expand over time.

12. Implications for the future

Future work is entirely open-ended. The development of specialised chips or helper tools for use with the bread-board is a deliberate feature of the system. Therefore third parties, or ourselves, can develop further features to extend the use of the toolsets into new areas. This is indeed the case at present, A Final year student has recently completed a new interface tool which allows industry standard tools such as Xilinx and Altera FPGA tools to generate designs to simulate on the Java BreadBoard. These Xilinx/Altera tools are available free as limited versions and use a methodology known as hardware description language (VHDL and VERILOG being the two key standards). Allowing the JBB tools to accept designs from this route opens up a wide range of new possibilities and applications as far as learning objectives are concerned.

Continuation of work with JBB at the University of York will be informal, as it must rely upon staff input without funding for the moment. However the approach of using final year projects as development vehicles is proven and useful. By making available the open source code, the

expectation is that this effort will multiply across the community and achieve a far greater collective impact than York alone.

There is limited funding available within the university for teaching innovation on a competitive basis: We would consider, in the future, running an event to bring together developers from the education community if enough activity is seen. A second possibility considered is to produce a textbook based on learning digital electronics, with the JBB tools as the experimental work-place for the student to build and work with circuits.

We expect to continue to support the JBB community web site at www.cs.york.ac.uk/jbb and hope that it will become a focus for a more active user-base in the future.

13. References

List any references to the work of others you have cited (e.g. articles, reports, studies, standards), and any explanatory notes. Provide URLs for any materials available on the web.

The original Java Bread-Board toolset is documented in Nicholas Glass's Final year report, available at :- http://www.cs.york.ac.uk/netpro/bboard/jbreadboard.pdf

14. Appendices

Glossary of Terms:-

Java	Programming language currently widely used.
Bread-Board	a circuit board designed for quick circuit building by use of plug-in chips and wires.
FPGA	Field Programmable Gate Array (a chip that can be reprogrammed to reproduce circuit behaviour)
VHDL	- a circuit description language
VERILOG	an alternative to VHDL with similar uses. (Verilog is favoured in the US, VHDL in Europe)
SourceForge	A repository for open-source program code

Following:-

Appendix 1: Conference Paper
Appendix 2: Gant Chart showing progress

APPENDIX 1a

Conference Paper

"**A JAVA Bread-Board Simulator : Digital Circuit Simulation with an Extensible Learning Tool"**,
Proceedings of **IADIS 2009** Applied Computing Conference, pp___, Rome, 2009,
Chris Bailey, Michael Freeman

APPENDIX 1b

Conference Paper

"Java Bread-Board :- Digital circuit simulation with an Open-source toolset",
IJCSIS (International Journal on Computer Science and Information Systems
IADIS ISSN: 1646-3692. Bailey, Freeman.
(Spring 2010 : accepted :- dates and final copy to be confirmed).,

APPENDIX 2

Project Gant Chart Showing progress as of 1st march 2010-03-02

A JAVA BREAD-BOARD SIMULATOR

Digital circuit simulation with an extensible e-learning tool

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ABSTRACT

Digital electronics is an area of student learning that benefits substantially from 'hands-on' experience. Simply simulating circuits at a high level will not instill a full understanding of the pitfalls involved in circuit building, testing, and design in the real world. Consequently most electronics related curriculums will include practical lab-work to supplement any other activities to be delivered as part of a course module. At many UK universities the use of 'bread-boards' is common. These are rapid circuit construction boards which allow circuits based upon chips to be wired and tested. However, it is less practical for students to undertake such work unsupervised (due to health and safety legislation), and also often not practical for them to undertake this work at home. Consequently, a Digital Bread Board simulator to supplement such teaching styles is a valuable teaching aid. This paper describes the Bread-Board Simulator developed at the University of York over a number of years, and a new project to release the tool-set as an Open-Source Learning Platform.

KEYWORDS

Digital Simulation, Bread-Board, Virtual Learning Environments, VHDL Simulation, Open-Source

1. INTRODUCTION

The use of bread-board circuit construction is a common methodology for practical digital electronics in UK universities. A Bread-Board is a circuit module that can have chips and wires inserted and removed without permanent fixing, and allows rapid construction and modification of test circuits. As such it presents an ideal medium for teaching of digital circuit design. However it is less convenient for students to make use of this medium at home or out of lab hours, and therefore students are limited to the amount of extra work they can do if seeking to learn at their own pace. This is especially so where increasing pressure to maximize utilization of lab facilities makes freelance access to facilities restrictive. Consequently, a learning tool that can be used on a computer platform as a supplementary learning tool, mirroring the functionality of a bread-board environment, was perceived to be a valuable goal by the first author. Subsequently, he established a series of student dissertation projects to develop the idea as an extensible platform for digital circuit experimentation – the Java Digital Bread-Board (JBB) was thus developed, and is described here in this publication.

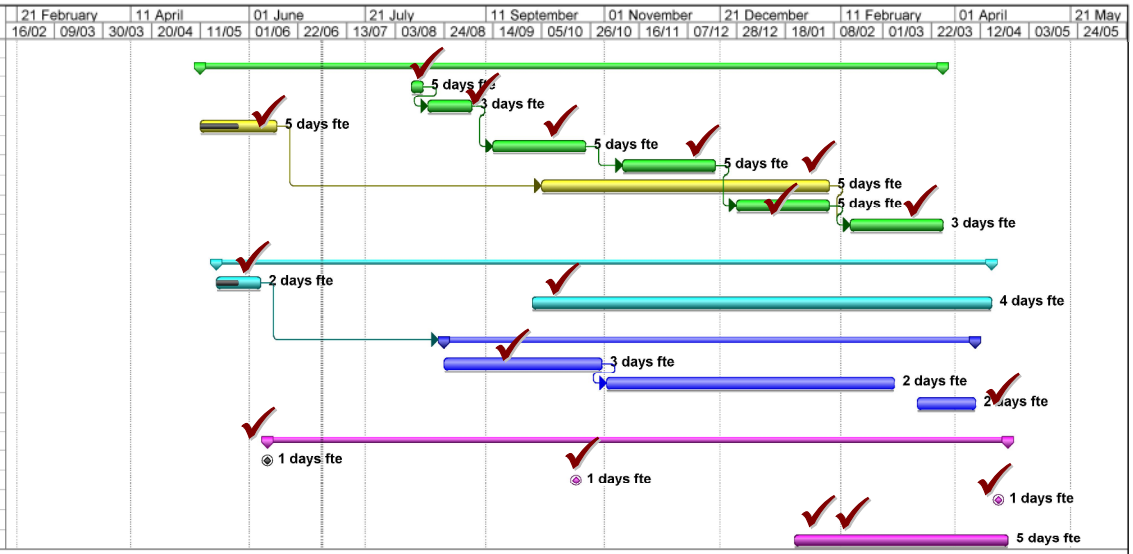
Please note that this paper describes in the authors own words, work undertaken over number of years by final year dissertation students under his direction, as per the acknowledgement at the end of this paper. It then discusses the further extension and future open-source development of the platform under a new project initiative. JBB was first evaluated in the EU Funded NETPRO Projects [Donazelli 1999, Bailey 2002], and has continued to be developed since.

2 JAVA BREAD-BOARD

The Bread-Board consists of a module (which may be interconnected to create multiples of larger size), upon which a series of interconnects are provided. Chips may be placed in the boards by inserting chip pins

Appendix-2 Project Gant Chart
Showing current completion of work-packages (01/03/2010)

ID	Task Name	Start	Finish	Resource Names
1				
2	**JBB Tool-Set Work**	**Mon 11/05/09**	**Fri 26/03/10**	
3	T1 Essential Training 10th Aug 5 days	Mon 10/08/09	Fri 14/08/09	5 days fte
4	I.1 JBB Appraisal	Mon 17/08/09	Fri 04/09/09	3 days fte
5	I.2 Evaluate alternative Platforms, obtain toolsets	Mon 11/05/09	Fri 12/06/09	5 days fte
6	S.1 Java Rebuild	Mon 14/09/09	Fri 23/10/09	5 days fte
7	S.2 Update Code & Documentation	Mon 09/11/09	Fri 18/12/09	5 days fte
8	S.2x Modify Code for portability (J2ME etc) if needed	Mon 05/10/09	Fri 05/02/10	5 days fte
9	S.3 Revise and Fix	Mon 28/12/09	Fri 05/02/10	5 days fte
10	S.4 Test and Validate	Mon 15/02/10	Fri 26/03/10	3 days fte
11				
12	**Open Source Community Site**	**Mon 18/05/09**	**Fri 16/04/10**	
13	I.2 Web research, Jorum Open Familiarisation	Mon 18/05/09	Fri 05/06/09	2 days fte
14	W.1 Update User Guide	Thu 01/10/09	Fri 16/04/10	4 days fte
15				
16	**W.2 Web-Site Spec, evaluate tools/options**	**Mon 24/08/09**	**Fri 09/04/10**	**2 days fte**
17	W.3a Web-Site Skeleton Implementation	Mon 24/08/09	Fri 30/10/09	3 days fte
18	W.3b Web-Site Content & Finishing	Mon 02/11/09	Fri 05/03/10	2 days fte
19	W.3c Coallate Addittional Learning Examples	Tue 16/03/10	Fri 09/04/10	2 days fte
20				
21	**HEA Requirements**	**Tue 09/06/09**	**Fri 23/04/10**	
22	HEFCE WORKSHOP	Tue 09/06/09	Tue 09/06/09	1 days fte
23	HEFCE WORKSHOP	Tue 20/10/09	Tue 20/10/09	1 days fte
24	HEFCE WORKSHOP	Tue 20/04/10	Tue 20/04/10	1 days fte
25				
26	D.1 Prepare Dissemination materials (papers/etc)	Fri 22/01/10	Fri 23/04/10	5 days fte



Project: Project v002
Date: Thu 02/07/09

Task | Progress | Summary | External Tasks | Deadline
Split | Milestone | Project Summary | External Milestone

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